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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,090	10/29/2003	Seung-Jae Chung	5649-1152	6639

7590 06/08/2006

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 06/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/696,090	CHUNG ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a non-Final Office Action in response to Amendment filed May 11, 2006. Claims 1-24 are presently under examination and still pending.

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d) for the REPUBLIC OF KOREA Application 2002-87246, filed 12/30/2002. The certified copy has been filed in parent Application No. 10/696,090, filed on 10/29/2003.

Objection to the abstract in the prior Office Action is now withdrawn in view of the amended abstract.

Rejection of Claims 1-12 under 35 U.S.C. 112, second paragraph, with respect to claims 1 and 4 for being indefinite, is hereby withdrawn in view of the Amendment to the claims and in view of Applicant's Remarks of clarification of the claimed invention.

Response to Arguments

Applicant's arguments, see Remarks filed May 11, 2006, with respect to the rejection of claims 1-24 under 35 U.S.C. 102(e) as being anticipated by Whetsel (US 6,877,122), have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made under 35 U.S.C. 102(e) as being anticipated by Song et al. (US 6,816,990), as set forth in the present Office Action, below.

In response to Applicant's argument, the Examiner agrees that Whetsel is silent with respect to performing "dynamic simulation testing". However, under a new ground

of rejection, Song recites in the independent claims 1 and 7 a method for performing "simulation testing" by shifting a plurality of pseudo random pulse patterns through at least one of the cores to detect faults in the at least one of the cores, by testing a combinational and sequential logic circuit with shift register latches of individual logic units coupled together to form a shift register scan path for testing logic circuits and uncoupled to disable the scan path while the logic circuit is performing its designed logic function.

Applicant's arguments with respect to claim 1-24 are moot in view of the new ground of rejection, as set forth in the present Office Action, below.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Song et al. (US Patent No. 6,816,990), filed: January 28, 2002.

Regarding independent Claims 1, 13, 15, 20, Song discloses a method and apparatus in Figure 5 for testing a circuit chip 500 provided with multiple cores and each core contains its own LBIST test structure like the one shown in Figure 4, comprising:

A core block configured for dynamic simulation testing by dividing the circuits into group cores, performing simulation testing by shifting a plurality of pseudo random pulse patterns through the cores to detect faults in the cores, and simultaneously performing simulation testing in other of the cores using a weighted pseudo-random pulse pattern, as recited by Song in the independent claims 1 and 7. The core block comprises multiple cores, core containing its own LBIST test structure as shown in Figure 4, having associated plurality of output ports corresponding to outputs of scan chains (402), for outputting test data into the multiple input shift register (MISR) 406.

An input side sub logic circuit unit, such as a linear feedback shift register (LFSR) 404 for configuring test patterns from a scan path for dynamic simulation testing. The (LFSR) 404 is coupled to the inputs of scan chains (402) through corresponding input multiplexers, as show in Figure 4. The LFSR generates the test patterns for loading the scan chain with random patterns and shifting the plurality of pseudo random pulse patterns through the cores to detect faults in the cores.

The input multiplexers, as show in Figure 4, are located between (LFSR) 404 and the input of scan chains (402) for selectively providing the test pattern from the (LFSR) 404 or the outputs from the scan chains 402, and wherein the core block generates output test data from the scan chains (402) outputs in response to test data from the input multiplexers.

Regarding independent Claims 4, 14, 16, 21, Song discloses a method and apparatus in Figure 5 for testing a circuit chip 500 provided with multiple cores and each core contains its own LBIST test structure like the one shown in Figure 4, comprising:

A core block configured for dynamic simulation testing by dividing the circuits into group cores, performing simulation testing by shifting a plurality of pseudo random pulse patterns through the cores to detect faults in the cores, and simultaneously performing simulation testing in other of the cores using a weighted pseudo-random pulse pattern, as recited by Song in the independent claims 1 and 7. The core block comprises multiple cores, core containing its own LBIST test structure as shown in Figure 4, having associated plurality of output ports corresponding to outputs of scan chains (402), for outputting test data into the multiple input shift register (MISR) 406. The core block having a plurality of output ports corresponding to outputs of scan chains (402) and a plurality of input ports corresponding to the inputs of scan chains (402) and a vector input SRI terminal (316) for introducing test data into scan chain circuit 300, Figure 3, and also shown as a serial input signal for introducing test data into (LFSR) 404 and multiplexer of scan chain (402) of Figure 4.

An input side sub logic circuit unit, such as a linear feedback shift register (LFSR) 404 for configuring test patterns from a scan path for dynamic simulation testing. The (LFSR) 404 is coupled to the inputs of scan chains (402) through corresponding input multiplexers, as show in Figure 4. The LFSR generates the test patterns for loading the scan chain with random patterns and shifting the plurality of pseudo random pulse patterns through the cores to detect faults in the cores.

The input multiplexers, as show in Figure 4, are located between (LFSR) 404 and the input of scan chains (402) for selectively providing the test pattern from the (LFSR) 404 or the outputs from the scan chains 402, and wherein the core block generates output test data from the scan chains (402) outputs in response to test data from the input multiplexers.

Regarding Claims 2, 5, Song discloses an output side sub logic circuit unit (multiple input shift register, MISR, 406) coupled to the outputs of scan chains (402) for receiving the test data for compression.

Regarding Claim 3, Song discloses wherein the MUX unit comprises a plurality of multiplexers coupled to the inputs of scan chains (402), respectively.

Regarding Claims 6-12, 17-19, 22-24, Song discloses scan chain (402, Figure 4) shown in detailed as scan chain (320, Figure 3). The data is introduced into the latches at shift register input (SRI) terminal 316 and transferred from one SRL to another to the shift register output (SRO) terminal. Then data is clocked into each SRL 300 by applying a clock pulse to master latch 308, and data is clocked out of each SRL 300 by applying a clock pulse to slave latch 310. Data is output from slave latch 310 to a succeeding master latch 308. The continuous, alternating application of a-clk and b-clk clock pulse signals on the a-clk and b-clk lines respectively sequentially propagates a data signal applied to SRI terminal 316 through scan chain 320 to SRO terminal 318. To effect a parallel load, a c.sub.1-clk block pulse is applied to c.sub.1-clk line. This causes a parallel load of data via parallel data inputs 302 and combinational logic to each master latch 308 of the SRLs 300, (see, col. 3, lines 28-60).

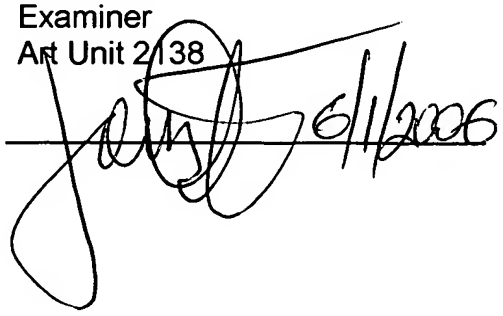
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JAMES C KERVEROS
Examiner
Art Unit 2138



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